(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 December 2001 (13.12.2001)

PCT

(10) International Publication Number
WO 01/95619 A2

(51) International Patent Classification[7]: H04N 5/74

(21) International Application Number: PCT/US01/18597

(22) International Filing Date: 7 June 2001 (07.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/210,284 8 June 2000 (08.06.2000) US

(71) Applicant: **DIGITAL REFLECTON, INC.** [US/US]; 644 University Avenue, Los Gatos, CA 95032 (US).

(72) Inventors: **FLASCK, Richard**; 10045 Nantucket, San Ramon, CA 94583-2865 (US). **SANDBERG, Edmund**; 17990 Rose Court, Monte Sereno, CA 95030 (US). **PRIOR, Gregory, A.**; 2814 Glen Heather Drive, San Jose, CA 95133 (US). **WEIHS, Paul, J.**; 37569 Summer Holly Common, Fremont, CA 94536 (US). **CACHARELIS, Philip, John**; 217 O'Connor, Menlo Park, CA 94025 (US).

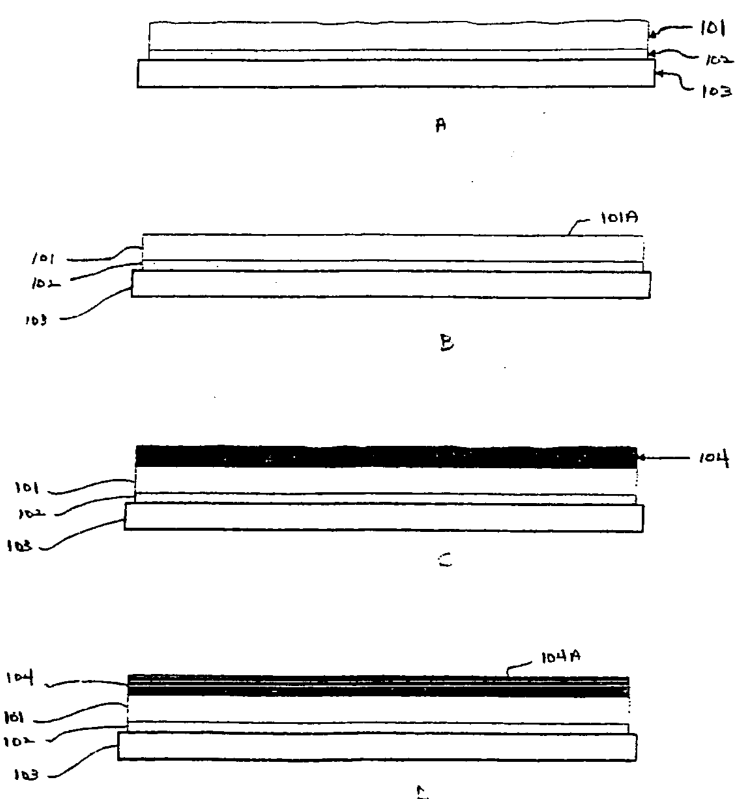
(74) Agent: **OH, Seong-Kun**; Sierra Patent Group, Ltd., P.O. Box 6149, Stateline, NV 89449 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: ACTIVE MATRIX SILICON SUBSTRATE FOR LCOS MICRODISPLAY BASED VIDEO PROJECTION APPLICATIONS



(57) Abstract: Method and system for providing improved performance of silicon substrate in a Liquid Crystal On Silicon (LCOS) microdisplay for use in video projection system with increased substrate reflectivity, reduced substrate scattering and diffraction, flicker suppression, minimized artifact of fringing and improved spatial uniformity of the gray scale, and allowing the substrate to operate in a high light environment is provided.

WO 01/95619 A2

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

SPECIFICATION

ACTIVE MATRIX SILICON SUBSTRATE FOR LCOS MICRODISPLAY BASED VIDEO PROJECTION APPLICATIONS

RELATED APPLICATION

The present application claims priority under 35 USC §119 to provisional application no. 60/210,284 filed on June 8, 2000.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to video projection systems. More particularly, the present invention relates to a silicon backplane in a microdisplay based video projection systems.

2. Description of the Related Art

The electrical and optical design of active matrix silicon substrate are major factors in determining the characteristics and quality of the video image produced by a microdisplay based video projection system. More specifically, a microdisplay may be used as the image source in a video projection system. The image on a Liquid Crystal On Silicon (LCOS) microdisplay is electrically controlled on a pixel-by-pixel basis by the active matrix silicon substrate. In this manner, the silicon substrate may be considered to be an electrically written, optically read analog DRAM. In particular, electrically, the silicon substrate contains an "analog pixel sampling and storage array" and "digital row/column addressing and control circuits."

Additionally, since the microdisplay is an optical component of the video projection system, the silicon substrate may also be required to have certain physical and optical properties. Some examples of these properties include surface of the pixels having high specular reflectivity accomplished by ensuring that the reflective surface is physically smooth

and highly reflective, as well as minimized diffraction from the silicon substrate. The interpixel gaps on the silicon substrate may be the source for the light loss mechanism responsible for the diffraction. In particular, differential reflection from the periodic variation in the physical structure forms a diffraction grating like structure.

Other desirable properties of the silicon substrate include an optically flat die. More specifically, since microdisplays are generally manufactured using a wafer-based process, the wafer itself must be optically flat. Lack of flatness may result in non-uniformity in the thickness of the liquid crystal layer. The non-uniformity, in turn, may result in fringing observed as band like variations in intensity in the projected image. Moreover, non-uniformity may cause variation in the electrical field which is observed as a variation in the shade of an image intended to have a uniform shade of gray.

If an exposed active matrix array is illuminated with high intensity light, undesirable photo-induced currents may be generated. Thus, it is desirable to shield the circuitry from incident light.

Furthermore, it is desirable that the silicon substrate operate at high frequency to eliminate flicker, which is a periodic and visible variation in the intensity of light reflected from the microdisplay under conditions where the desired output is steady. Although several mechanisms may contribute to the occurrence of flicker, the primary source of flicker may be an asymmetry in the internal materials of the microdisplay. By increasing the frame rate at which the silicon substrate is operated, the flicker may be removed from the visibility of human eye.

Other properties to be considered for designing the silicon substrate in the LCOS microdisplay include the vertical and horizontal pixel count, the aspect ratio of the active matrix array, the format or system by which the image is presented on the display, the number of analog gray scale levels that the substrate can support, and the voltage that the substrate can apply to the liquid crystal layer. In particular, regarding the vertical and horizontal pixel count, the resolution of the active matrix array may be any size including VGA, SVGA, XGA, UXGA, 1920x1080, or 1920x1200. Moreover, the aspect ratio may be

any shape including 16:9, 16:10, 5:4, or 4:3.

The format or system by which the image is presented on the display may be interlaced or progressive, while the number of analog gray scale levels that the substrate can support may be any value (for example, a microdisplay design which produces 10 bits or 1024 levels). Finally, regarding the voltage that the substrate can apply to the liquid crystal layer, the amplitude of the available high voltage generally determines the range of the liquid crystal optical effects that the substrate can support. Additionally, the voltage is the determining factor in the response speed of the microdisplay and in the blackness of the dark state image.

SUMMARY OF THE INVENTION

In view of the foregoing, a pixel array for use in a microdisplay of a video projection system in accordance with one embodiment of the present invention includes a substrate layer, an underlying layer deposited on the substrate layer, a dielectric layer deposited on the underlying layer, the dielectric layer polished to provide a substantially smooth upper surface, and a metal layer deposited on the polished smooth upper surface of the dielectric layer, the metal layer polished to provide a substantially smooth upper surface.

The substrate layer may include a silicon substrate layer, and the metal layer may include an aluminum layer.

The upper surface of said metal layer may be polished using chemical mechanical polishing, where polished substantially smooth upper surface of the metal layer is configured to provide a high specular reflectivity.

A pixel array for use in a microdisplay of a video projection system in accordance with another embodiment of the present invention include a substrate layer, an underlying layer deposited on the substrate layer, a dielectric layer deposited on the underlying layer, said dielectric layer etched on an upper surface to form a plurality of pixel grooves, a metal layer deposited on the etched upper surface of said dielectric layer, said metal layer polished to provide a substantially smooth upper surface such that said metal layer is provided in said

pixel grooves and an interpixel gap of said dielectric layer is provided between each adjacent pixel groove.

The dielectric layer may be substantially transparent, and may have a high breakdown voltage.

A pixel array for use in a microdisplay of a video projection system in accordance with yet another embodiment of the present invention includes a substrate layer, an underlying layer deposited on said substrate layer, a dielectric layer deposited on said underlying layer, a metal layer deposited on said dielectric layer, and a reflection enhancing layer deposited on said metal layer.

The reflection enhancing layer may include a coating comprising a stack of thin films.

The stack of thin films may include a first silicon dioxide layer deposited on said metal layer, a silicon nitride layer deposited on said first silicon dioxide layer, a second silicon dioxide layer deposited on said silicon nitride layer.

Furthermore, each of said first and second silicon dioxide layers and said silicon nitride layer may have a thickness of half the wavelength of light divided by an index of refraction of the corresponding layers.

An active pixel matrix array for use in a microdisplay of a video projection system in accordance with still another embodiment of the present invention includes a predetermined number of columns including even numbered columns and odd numbered columns, each of said even numbered columns configured to receive a first input, and each of said odd numbered columns configured to receive a second input, and a predetermined number of rows, said columns and rows together forming said array.

The predetermined number of columns may be 1920 and said predetermined number of rows may be 1080.

The even numbered columns may include 960 columns and said odd numbered columns may include 960 columns, each of said even numbered columns being adjacent to a respective odd numbered column.

The first and second inputs may respectively include a voltage signal having a

predetermined phase, the predetermined phase may be either 90 or 180 degrees out of phase.

Furthermore, a seal ring may be provided substantially around the outer periphery of said array, a plurality of alignment targets being provided substantially between said array and said seal ring.

Each of the alignment target may have an inner width of one micron with a total length of 10 microns, and may be respectively provided between the four outer corners of said array and the four inner corners of said array.

Moreover, the array may further include an additional set of rows provided on both left and right sides of said array and an additional set of columns provided on both upper and lower sides of said array, thus providing a larger array.

The image area of a projected video image may be provided within said larger array.

An active pixel matrix array for use in a microdisplay of a video projection system in accordance with still yet a further embodiment of the present invention includes a predetermined number of columns including a first group of columns numbered (1+4n), a second group of columns numbered (3+4n), a third group of columns numbered (2+4n), and a fourth group of columns numbered (4+4n), each of said first, second, third and fourth group of columns configured to receive a separate respective first, second, third and fourth inputs, said n being a positive integer including zero, and a predetermined number of rows, said columns and rows together forming said array.

The predetermined number of columns may be 1920 and said predetermined number of rows may be 1080. Additionally, each of said first, second, third, and fourth group of columns may include 480 columns.

An active pixel matrix array for use in a microdisplay of a video projection system of another aspect of the present invention includes a predetermined number of columns, said columns divided into an upper section and a lower section, and a predetermined number of rows, said columns and rows together forming said array.

The upper section columns may be configured to address a first group of rows and said lower section columns may be configured to address a second group of rows, said first

and second group of rows comprising said predetermined number of rows.

The predetermined number of columns may be 1920 and said predetermined number of rows may be 1080.

The predetermined columns may be divided substantially in the middle such that each of said upper section columns and each of said lower section columns have substantially the same length.

The predetermined number of rows may be divided into a left section and a right section, and the left section rows may include 540 rows and said right section rows may include 540 rows.

Further, a first portion of said upper section columns may be configured to address a first portion of said left section rows, a first portion of said lower section columns may be configured to address a second portion of said left section rows, a first portion of said lower section columns may be configured to address a first portion of said right section rows, and a second portion of said lower section columns may be configured to address a second portion of said right section rows.

The first and second portions of said upper section columns may be non-overlapping, said first and second portions of said lower section columns may be non-overlapping, said first and second portions of said left section rows may be non-overlapping and said first and second portions of said right section rows may be non-overlapping.

The first and second portions of said upper section columns may each include 960 columns, said first and second portions of said lower section columns may each include 960 columns, said first and second portions of left section rows may each include 540 rows, and further, said first and second portions of said right section rows may each include 540 rows.

A method of providing a pixel array for use in a microdisplay of a video projection system of one aspect of the present invention includes depositing an underlying layer on a substrate layer, depositing a dielectric layer on said underlying layer and polishing said dielectric layer to provide a substantially smooth upper surface, and depositing a metal layer on said polished smooth upper surface of said dielectric layer and polishing said metal layer

to provide a substantially smooth upper surface.

A method of providing a pixel array for use in a microdisplay of a video projection system of another aspect of the present invention includes depositing an underlying layer on a substrate layer, depositing a dielectric layer on said underlying layer and etching said dielectric layer on an upper surface to form a plurality of pixel grooves, depositing a metal layer on said etched upper surface of said dielectric layer and polishing said metal layer to provide a substantially smooth upper surface such that said metal layer is provided in said pixel grooves and an interpixel gap of said dielectric layer is provided between each adjacent pixel groove.

A method of providing a pixel array for use in a microdisplay of a video projection system of yet another aspect of the present invention includes depositing an underlying layer on a substrate layer, depositing a dielectric layer on said underlying layer, depositing a metal layer on said dielectric layer, and depositing a reflection enhancing layer on said metal layer.

The reflection enhancing layer depositing step may include the steps of depositing a first silicon dioxide layer on said metal layer, depositing a silicon nitride layer on said first silicon dioxide layer, depositing a second silicon dioxide layer on said silicon nitride layer.

A method of providing an active pixel matrix array for use in a microdisplay of a video projection system of still another aspect of the present invention includes providing a predetermined number of columns including even numbered columns and odd numbered columns, each of said even numbered columns configured to receive a first input, and each of said odd numbered columns configured to receive a second input, and providing a predetermined number of rows, said columns and rows together forming said array.

A method of providing an active pixel matrix array for use in a microdisplay of a video projection system of yet still another aspect of the present invention includes dividing a predetermined number of columns into an upper section and a lower section, and providing a predetermined number of rows, said columns and rows together forming said array.

In the manner described above, in accordance with the various embodiments of the present invention, improved performance of silicon substrate in a Liquid Crystal On Silicon

(LCOS) microdisplay for use in video projection system is provided. In particular, the LCOS microdisplay of the various embodiments of the present invention provides increased substrate reflectivity, reduced substrate scattering and diffraction, flicker suppression, minimized artifact of fringing and improved spatial uniformity of the gray scale, as well as allowing the substrate to operate in a high light environment.

These and other features and advantages of the various aspects and embodiments of the present invention will be understood upon consideration of the following detailed description of the invention and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1D illustrate one approach for providing physically smooth pixel surface in the active pixel array in accordance with one embodiment of the present invention.

Figures 2A-2D illustrate one approach for filling the interpixel gap to minimize diffraction from the silicon substrate in accordance with one embodiment of the present invention.

Figure 3 illustrates one approach for increasing pixel reflectivity in accordance with one embodiment of the present invention.

Figures 4A-4B illustrate approaches for configuring the pixel array to support a higher frame rate in accordance with one embodiment of the present invention.

Figure 5 illustrates one approach for increasing the operating voltage applied by the active pixel array in accordance with one embodiment of the present invention.

Figures 6A-6C illustrate waveforms for driving the pixels in the active pixel array in accordance with one embodiment of the present invention.

Figure 7 illustrates a circuit schematic for generating a phase shifted waveform for driving the pixels shown in Figure 6A-6C.

Figures 8A-8B illustrate one approach for assisting the alignment of microdisplays on the prism in accordance with one embodiment of the present invention.

Figure 9 illustrates one approach for centering and/or aligning the projected image on

the screen in a video projection system in accordance with one embodiment of the present invention.

Figure 10 illustrates one approach for providing improved active matrix silicon yield and reliability in the microdisplay based video projection system in accordance with one embodiment of the present invention.

Figures 11A-11B illustrate one approach for providing reduced resistance and/or capacitance of the traces in the active matrix array in accordance with one embodiment of the present invention.

INCORPORATION BY REFERENCE

What follows is a cite list of references each of which is, in addition to those references that may be cited above and below herein, including that which is described as background, and the above invention summary, are hereby incorporated by reference into the detailed description of the preferred embodiment below, as disclosing alternative embodiments of elements or features of the preferred embodiments not otherwise set forth in detail below. A single one or a combination of two or more of these references may be consulted to obtain a variation of the preferred embodiments described in the detailed description below. Further patent, patent application and non-patent references may be cited in the written description and are also incorporated by reference into the detailed description of the preferred embodiment with the same effect as just described with respect to the following references:

United States patent applications no. 60/192,258, 60/192,732, 60/194,735, 60/198,436, 60/200,094, 60/202,265, 60/208,603, 60/210,784, 60/210,285, 60/213,334, 60/214,574, 60/215,932, 60/217,758, 60/220,979, 60/224,617, 60/224,961, 60/224,257, 60/224,503, 60/224,291, 60/224,290, 60/224,060, 60/224,059, 60/224,061, 60/224,289, 60/227,229, 60/229,666, 60/230,330, 60/230,326, 60/232,281, 60/234,415, 60/245,807 and 60/249,815, each of which is assigned to the same assignee as the present application.

DETAILED DESCRIPTION OF THE INVENTION

Figures 1A-1D illustrate one approach for providing physically smooth pixel surface in the active pixel array in accordance with one embodiment of the present invention. Referring to Figure 1A, as shown, a dielectric layer 101 is deposited on a silicon substrate 103, with underlying layers 102 provided therebetween. Referring to Figure 1B, the upper surface 101a of the dielectric layer 101 is smoothed using Chemical Mechanical Polishing (CMP) to physically smooth the deposited dielectric layer 101. Thereafter, referring to Figure 1C, the top metal pixel electrode 104 which, in one embodiment, may be a layer of aluminum, is deposited on the smoothed upper surface 101a of the dielectric layer 101. Then, the upper surface 104a of the deposited top metal pixel electrode layer 104 is polished using Chemical Mechanical Polishing as shown in Figure 1D.

In this manner, in accordance with one embodiment of the present invention, a mirror like pixel electrode surface may be achieved providing for a specularly reflective active pixel array by, for example, physically smoothing the top metal pixel electrodes. Accordingly, the surface of the pixels may have high specular reflectivity having a reflective surface which are both physically smooth and highly reflective.

Figures 2A-2D illustrate one approach for filling the interpixel gap to minimize diffraction from the silicon substrate in accordance with one embodiment of the present invention. Referring to Figure 2A, similar to the illustration shown in Figure 1A, a layer of dielectric 101 is deposited on the silicon substrate 103 with the underlying layers 102 therebetween. Then, the deposited dielectric layer 101 is etched from the pixels as shown in Figure 2B such that the etched dielectric layer 101a is provided with pixel grooves 101b with interpixel gap 101c therebetween. Referring to Figure 2C, the top metal pixel electrode layer 104 such as aluminum is deposited on the etched dielectric layer 101a. Finally, as shown in Figure 2D, the Chemical Mechanical Polishing (CMP) is used to polish the surface of the etched dielectric layer 101a deposited with the top metal pixel electrode layer 104, providing a polished upper surface of the etched dielectric layer 101d forming the upper surface of the interpixel gap between the pixels 101e.

In the manner described above, in accordance with one aspect of the present invention, the gap filling material may be selected to provide good electrical insulation. Moreover, the CMP procedure assures that the surface is smooth. Further, if the gap filling material is inherently reflective, the reflectivity of the interpixel gap may be provided to be similar to the pixel to prevent a periodic variation in reflectivity, since such variation may be the source of diffraction which can be a significant light loss mechanism. In one embodiment, the gap filling material may be of transparent material in which case the light is transmitted through the gap filling material to be reflected by the metal layer of the underlying layers 102. Accordingly, in one aspect, the interpixel gap material has a high breakdown voltage to prevent electrical shorting between the pixels, thus providing insulation between the adjacent pixels. Moreover, the uppermost surface of the active pixel array is smoothed to provide uniform alignment of the liquid crystal. Additionally, as discussed above, the reflectivity of the interpixel gap is provided to be similar to the pixel such that the periodic variation in reflectivity may be prevented.

Figure 3 illustrates one approach for increasing pixel reflectivity in accordance with one embodiment of the present invention. Referring to Figure 3, a reflection enhancing layer is provided on the polished top metal pixel electrode layer 104. In particular, a layer of silicon dioxide 301 is deposited on the polished top metal pixel electrode layer 104, and a layer of silicon nitride 302 is deposited on the layer on silicon dioxide 301. Finally, another silicon dioxide layer 303 is deposited on the layer of silicon nitride 302. In this manner, the stack of thin films comprising the silicon dioxide 310 - silicon nitride 302 - silicon dioxide 303 together forms the reflection enhancing coating. In one embodiment, this thickness of each layer may be half the wavelength of the light in air divided by the index of refraction of the layer material.

In this manner, in one aspect of the present invention, pixel reflectivity may be enhanced by providing a reflection enhancing coating. In particular, since aluminum is generally used as the reflective surface in a microdisplay in video projection systems, and the inherent reflectivity of aluminum is typically in the low 80%, by providing the reflection

enhancing layer as discussed above, the pixel reflectivity may be enhanced, thus providing for a high specular reflectivity. Additionally, since the reflection enhancing layer 301-303 is deposited on the top metal electrode 104, the surface of these deposited thin films 301-303 will also be the substrate for the liquid crystal alignment layer. Furthermore, since the liquid crystal alignment layer needs to be planarized, the thin films of the reflection enhancing layer 301-303 will provide the smooth underlying surface necessary for an alignment layer.

Figures 4A-4B illustrate approaches for configuring the pixel array to support a higher frame rate in accordance with one embodiment of the present invention. Referring to Figure 4A, one embodiment for providing higher frame rate for addressing active matrix array is shown. In particular, as shown in the Figure, the columns of the active matrix array are separately addressed from the top and the bottom. More specifically, the odd columns 401 of the 960 columns in the active matrix array shown in Figure 4A is addressed with a first data input IP1, while the even columns 402 of the 960 columns in the active matrix array are addressed from the bottom of the array by a second data input IP2, thus comprising a two-phase addressing.

Referring to Figure 4B, a second embodiment for providing higher frame rate for addressing active matrix array is shown. In particular, in the four-phase addressing shown in Figure 4B, while the odd columns of the active matrix array are addressed from the top and the even columns are addressed from the bottom similar to the embodiment shown in Figure 4A, as shown, two separate input addresses are provided for each of the odd and even columns in the active matrix array. More particularly, a first data input IP1 is configured to address 480 odd columns 411a in the active matrix array having column numbers (1+4n), while a second data input IP2 is configured to address a second group of 480 odd columns 411b having column numbers (3+4n), where n is an integer. Moreover, a third data input IP3 is configured to address a first group of 480 even columns 412a in the active matrix array having column numbers (2+4n), while a fourth data input IP4 is configured address a second group of 480 even columns 412b having column numbers (4+4n), where n is an integer.

As discussed above, visible flicker is generally unacceptable in a consumer video

product. The origin of the flicker relates to the physical construction of the microdisplay, and while it may be possible to minimize the flicker by using improved configurations in the microdisplays, a more effective approach may be to increase the frame rate which is the frequency at which the image is updated. The flicker in a typical 60 Hz LCOS based video system occurs at every 30 Hz (i.e., half the frame rate), and falls within a frequency range to which the eye is especially sensitive. Accordingly, increasing the frequency significantly reduces the visibility of the flicker. With increase in the range of 70 to 90 Hz, observable flicker is reduced, however, driving a microdisplay at a frame rate in this range also introduces unwanted artifacts. The unwanted artifacts are derived from the unequal rate at which the video data is being fed into and drawn from the buffer. In other words, the data output to each sub-frame has not had sufficient time to be completely updated and is manifested as "stutter" and/or "tear" in the video image. In view of the above, the present invention in one aspect increases the frame rate to double the usual video rate such that the video data is input to the buffer at 60 Hz and the video data is output at 120 Hz with the same fully available data supplied to each sub-frame.

In particular, the two phase and four-phase addressing approaches of the present invention provide increased number of inputs that effectively lowers the transmission bandwidth requirements, and thus increasing the refresh rate that can be applied to the active matrix array. Since using a single data input path to address all 1920 columns of the array at a frame rate of 120 Hz is impractical with the existing data transmission rate approaches, in the manner described above, in accordance with the various embodiments of the present invention, the microdisplay may be configured to operate at a higher frame rate by for example, implementing the two-phase or four-phase addressing discussed above.

Figure 5 illustrates one approach for increasing the operating voltage applied by the active pixel array in accordance with one embodiment of the present invention. Referring to Figure 5, the pixel access transistor 500 is provided with a drift region 502 which, in one embodiment, may be laterally extended by increasing the lateral extent of the drift region 502 to the extended position 501. Alternatively, the depth of the drift region 502 may be

increased to similarly increase the operating voltage to a sufficiently high level for the microdisplay.

Indeed, as shown, in one embodiment of the present invention, the drift region of the pixel access transistor is extended by increasing the depth of the drift region or by increasing the lateral extent of the drift region as shown in the Figure. In this manner, the substrate may be configured to increase the produced operating voltage sufficiently high to meet the needs of any liquid crystal optical effect that may be incorporated into the microdisplay.

Figures 6A-6C illustrate waveforms for driving the pixels in the active pixel array in accordance with one embodiment of the present invention. Referring to Figures 6A-6C, waveforms applied to the column and rows at a frequency sufficiently high to render flicker invisible to the human eye are shown. As shown, the amplitude of the waveforms shown in Figures 6A-6C are substantially fixed, and the RMS voltage applied to each pixel is determined by the phase relationship between the transparent conductor Iridium Tin Oxide (ITO) and the respective pixel waveforms.

More specifically, Figure 6A illustrates the case where the waveforms are in phase and the RMS voltage is zero, while Figure 6B illustrates the case where the waveforms are 90 degrees out of phase and the RMS voltage is half of the maximum, and lastly, Figure 6C illustrates the case where the waveforms are 180 degrees out of phase and the applied RMS voltage is maximized. Accordingly, intermediate voltage levels may be developed to drive the shades of gray. Thus, in accordance with one aspect of the present invention, flicker free images may be produced, while minimizing artifacts that may appear from the translation of the input video signal to the pixel drive waveform using design circuitry that can be implemented with current silicon technology.

Figure 7 illustrates a circuit schematic for generating a phase shifted waveform for driving the pixels shown in Figure 6A-6C. Referring to Figure 7, as shown, there is provided a comparator 701 configured to receive the video input at its positive input terminal 701A and the sawtooth input signal at its negative input terminal 701B. Also coupled to the positive input terminal 701A of the comparator 701 is a electronic circuit schematic 702 of

the liquid crystal pixels. The output of the comparator 701 is provided to an exclusive OR gate 703 which is also configured to receive the ITO signal. As further shown in the Figure, the output of the exclusive OR gate 703 is coupled with a capacitor Cpixel, the opposite side of which is provided with the ITO signal. In this manner, in accordance with one embodiment of the present invention, a circuit configuration for generating the phase shifted waveform for driving the pixels shown in Figure 6A-6C is provided.

Figures 8A-8B illustrate one approach for assisting the alignment of microdisplays on the prism in accordance with one embodiment of the present invention. In particular, Figure 8A illustrates one embodiment of the optical alignment targets positioned in the top metal layer of silicon, the targets being holes in the metal layer, while Figure 8B illustrates one embodiment of the optical alignment target in accordance with the present invention. More specifically, referring to Figure 8A, the optical alignment targets 810 are positioned within the metal layer 840 at the four corners between the active array 820 and the seal ring 830.

Referring to Figure 8B, it can be seen that the dimensions of the optical alignment target 810 in one embodiment is approximately 10 microns in length and width, relative to the top metal layer 840 shown in Figure 8B with a height of 20 microns to the edge of the seal ring 830, for example, in the case the alignment target 810 is positioned at the top left corner in Figure 8A. Moreover, the lines running through the alignment target 810 as shown in Figure 8B in one embodiment may have a width W of 1 micron. In this manner, in one aspect, the red, green and blue microdisplays may be automatically aligned along their X, Y and rotational axes with +/- 2 microns in required tolerance as they are mounted on the prism assembly. Thus, the microdisplays in a high volume production of a video projection system with multiple color channels may be accurately aligned.

Figure 9 illustrates one approach for centering and/or aligning the projected image on the screen in a video projection system in accordance with one embodiment of the present invention. Referring to Figure 9, for an image area 910 of the active matrix array 920, extra rows and/or columns 930 may be added to the active matrix array 920. In this manner, the image can be electronically shifted within the active matrix array 920 in the vertical and/or

horizontal directions.

In particular, when a light train projects a video image onto a screen, it is important that the image be properly centered on the screen. One approach to center the projected image on the screen is to physically adjust the position of the light train with respect to the other components in the projection system which may include, among other things, an enclosure or housing, mirrors and the screen. While a desired may be achieved in this approach, such multi-axis physical adjustment may be difficult, time consuming or expensive to implement when a large number of such projection systems are produced. Accordingly, the centering and alignment approach of the projected image on the screen in accordance with one embodiment of the present invention described above provides for electronically shifting the image area 910 within the active matrix array 920 by using extra rows and/or columns 930 which effectively provide greater active matrix array 920 for shifting the image area 910.

Figure 10 illustrates one approach for providing improved active matrix silicon yield and reliability in the microdisplay based video projection system in accordance with one embodiment of the present invention. Referring to Figure 10, three feed throughs are provided as shown as compared with a single feed through. In this manner, in accordance with one embodiment of the present invention, the yield and reliability of the active matrix silicon substrate may be improved by increasing (for example, tripling) the number of buried contacts between the pixel-input transistor and the storage capacitor.

Figures 11A-11B illustrate one approach for providing reduced resistance and/or capacitance of the traces in the active matrix array in accordance with one embodiment of the present invention. Referring to Figure 11A, as shown, there are provided 1920 columns and 1080 rows extending across the entire active matrix array. Further shown in Figure 11A are the 1920 columns split in the center of the array such that 1920 columns address the top 540 rows and another 1920 columns address the bottom 540 rows. In this manner, by reducing the length of the columns, both the capacitance and the resistance may be reduced. As a trade off, additional connections are necessary for implementing such design.

Referring to Figure 11B, as can be seen, the 1080 rows may be split in the center of

the matrix in addition to the 1920 columns such that 860 columns in the top left of the matrix array are configured to address the 540 rows at the top left of the matrix array, the 860 columns in the top right of the matrix array are configured to address the 540 rows at the top right of the matrix array, the 860 columns in the bottom left of the matrix are configured to address the 540 rows at the bottom left of the matrix array, and finally, the 860 columns in the bottom right of the matrix array are configured to address the 540 rows at the bottom right of the matrix array.

Indeed, in a large and dense active matrix array, the length of the traces may become long, and the width of the traces may become narrow, both of which being attributable to an increase in the resistance and capacitance of the traces, requiring more power to drive the array. Additionally, transmission line delays may be introduced that may distort the image. Accordingly, in the various aspects of the present invention discussed above, by reducing the length of the columns and/or the rows of the active matrix array, the capacitance and the resistance of the traces may be reduced.

The LCOS microdisplay must have a uniform cell gap defined as the spacing between the cover glass and the silicon substrate. The cell gap is generally filled with a layer of liquid crystal material. During manufacturing processes, producing a uniform cell gap requires that the cell assembly procedure not introduce any non-uniform stress and that the silicon substrate be relatively flat. In view of the foregoing, in one aspect of the present invention, using a tool such as that available from SEZ Corporation, the thin film coatings from the back of the wafer is removed such that flat active matrix silicon wafers and dies may be obtained to achieve a uniform cell gap in the LCOS microdisplay.

Accordingly, an optically flat silicon wafer and die may be obtained such that fringing in the projected image as well as variations in the shades of the image is minimized.

Furthermore, as discussed above, when an "exposed" active matrix array is illuminated with high intensity light, undesirable photo-induced currents may be generated. Thus, in various aspects of the present invention, techniques for shielding the circuitry particularly the transistors from incident light is disclosed. More specifically, using the top

metal pixel electrode, the metal of the ground layer, and to a lesser extent, the metal 1 traces as a light shield. In one embodiment, the metal of the ground layer and the metal 1 may be within the "underlying" layers as shown in Figure 1A. The layers may be staggered such that the incoming incident light may be substantially prevented from direct illumination of the transistor array of the active pixel matrix.

In another approach, the dielectric layer 101 (Figure 1A) may be chosen with light absorbing properties. In this manner, any lateral transmission of scattered light may be prevented. In yet another approach, since the dielectric layer 101 (Figure 1A) deposited between the metal layers 104 and 102 forms an optical transmission line, by modifying the thickness of the dielectric layer 101, a transmission line that has a destructive interference may be obtained to prevent lateral transmission of light. While several separate approaches to preventing high intensity light from reaching the transistors of the pixel array is discussed above, in one aspect of the present invention, these approaches may be employed in combinations for a single silicon substrate to obtain shielding from high intensity light.

In a further aspect of the present invention, to provide optimization of microdisplay products for different applications in an efficient and cost effective manner, active matrix silicon substrate that can support a variety of different operating modes is disclosed. In particular, the active matrix silicon substrate may be configured to accommodate differing optical effect and applied voltage relationships each specific to the various liquid crystal display configurations for LCOS microdisplay based projection systems. By providing a sufficiently high operating voltage of the active matrix silicon substrate to drive the respective liquid crystal configurations with the highest voltage requirements, for example, as discussed above with respect to the embodiment shown in Figure 5, the respective liquid crystal configurations may be provided with sufficient voltage for the intended applications.

Referring again to LCOS microdisplays, the electro-optical response of microdisplays generally varies with temperature. Thus, it may be desirable to adjust the voltages applied to the microdisplays as a function of temperature, or alternatively, it may be desirable to control the temperature of the microdisplay itself. Whether in the case of adjusting the voltages

based on the temperature or controlling the temperature itself of the microdisplay, the temperature of the microdisplay must be accurately detected or sensed. In one aspect of the present invention, a temperature-sensing component may be added to the active matrix silicon substrate backplane, with the connections to the temperature sensing component bonded to the boding pad ledge. In this manner, the temperature of the microdisplay may be accurately sensed for voltage adjustment or temperature control of the microdisplay.

In the manner described above, in accordance with the various embodiments of the present invention, improved performance of silicon substrate in a Liquid Crystal On Silicon (LCOS) microdisplay for use in video projection system is provided. In particular, the LCOS microdisplay of the various embodiments of the present invention provides increased substrate reflectivity, reduced substrate scattering and diffraction, flicker suppression, minimized artifact of fringing and improved spatial uniformity of the gray scale, as well as allowing the substrate to operate in a high light environment.

Various other modifications and alterations in the structure and method of operation of this invention will be apparent to those skilled in the art without departing from the scope and spirit of the invention. Although the invention has been described in connection with specific preferred embodiments, it should be understood that the invention as claimed should not be unduly limited to such specific embodiments. It is intended that the following claims define the scope of the present invention and that structures and methods within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A pixel array for use in a microdisplay of a video projection system, comprising:

a substrate layer;

an underlying layer deposited on said substrate layer;

a dielectric layer deposited on said underlying layer, said dielectric layer polished to provide a substantially smooth upper surface; and

a metal layer deposited on said polished smooth upper surface of said dielectric layer, said metal layer polished to provide a substantially smooth upper surface.

2. The array of claim 1 wherein said substrate layer includes a silicon substrate layer.

3. The array of claim 1 wherein said metal layer includes an aluminum layer.

4. The array of claim 1 wherein said upper surface of said metal layer is polished using chemical mechanical polishing.

5. The array of claim 1 wherein said polished substantially smooth upper surface of said metal layer is configured to provide a high specular reflectivity.

6. The array of claim 1 wherein said underlying layer includes a ground metal layer.

7. A pixel array for use in a microdisplay of a video projection system, comprising:

a substrate layer;

an underlying layer deposited on said substrate layer;

a dielectric layer deposited on said underlying layer, said dielectric layer etched on an upper surface to form a plurality of pixel grooves; and

a metal layer deposited on said etched upper surface of said dielectric layer, said metal layer polished to provide a substantially smooth upper surface such that said metal

layer is provided in said pixel grooves and an interpixel gap of said dielectric layer is provided between each adjacent pixel groove.

8. The array of claim 7 wherein said substrate layer includes a silicon substrate layer.

9. The array of claim 7 wherein said metal layer includes an aluminum layer.

10. The array of claim 7 wherein said upper surface of said metal layer is polished using chemical mechanical polishing.

11 The array of claim 7 wherein said dielectric layer is substantially transparent.

12. The array of claim 11 wherein said dielectric layer has a high breakdown voltage.

13. The array of claim 7 wherein said underlying layer includes a ground metal layer.

14. A pixel array for use in a microdisplay of a video projection system, comprising:
a substrate layer;
an underlying layer deposited on said substrate layer;
a dielectric layer deposited on said underlying layer;
a metal layer deposited on said dielectric layer; and
a reflection enhancing layer deposited on said metal layer.

15. The array of claim 14 wherein said substrate layer includes a silicon substrate layer.

16. The array of claim 14 wherein said metal layer includes an aluminum layer.

17. The array of claim 14 wherein said reflection enhancing layer includes a coating

comprising a stack of thin films.

18. The array of claim 17 wherein said stack of thin films includes:

a first silicon dioxide layer deposited on said metal layer;

a silicon nitride layer deposited on said first silicon dioxide layer; and

a second silicon dioxide layer deposited on said silicon nitride layer.

19. The array of claim 18 wherein each of said first and second silicon dioxide layers and said silicon nitride layer has a thickness of half the wavelength of light divided by an index of refraction of said corresponding layers.

20. An active pixel matrix array for use in a microdisplay of a video projection system, comprising:

a predetermined number of columns including even numbered columns and odd numbered columns, each of said even numbered columns configured to receive a first input, and each of said odd numbered columns configured to receive a second input; and

a predetermined number of rows, said columns and rows together forming said array.

21. The array of claim 20 wherein said predetermined number of columns is 1920 and said predetermined number of rows is 1080.

22. The array of claim 20 wherein said even numbered columns includes 960 columns and said odd numbered columns includes 960 columns, each of said even numbered columns adjacent to a respective odd numbered column.

23. The array of claim 20 wherein said first and second inputs are the same.

24. The array of claim 20 wherein said first and second inputs respectively include a

voltage signal having a predetermined phase.

25. The array of claim 24 wherein said predetermined phase is 90 degrees out of phase.

26. The array of claim 24 wherein said predetermined phase is 180 degrees out of phase.

27. The array of claim 20 further including a seal ring provided substantially around the outer periphery of said array, a plurality of alignment targets provided substantially between said array and said seal ring.

28. The array of claim 27 wherein each of said alignment target has an inner width of one micron with a total length of 10 microns.

29. The array of claim 27 wherein each of said plurality of alignment targets is respectively provided between the four outer corners of said array and the four inner corners of said array.

30. The array of claim 20 further including an additional set of rows provided on both left and right sides of said array and an additional set of columns provided on both upper and lower sides of said array, providing a larger array.

31. The array of claim 30 wherein an image area of a projected video image is provided within said larger array.

32. An active pixel matrix array for use in a microdisplay of a video projection system, comprising:

a predetermined number columns including a first group of columns numbered (1+4n), a second group of columns numbered (3+4n), a third group of columns numbered

(2+4n), and a fourth group of columns numbered (4+4n), each of said first, second, third and fourth group of columns configured to receive a separate respective first, second, third and fourth inputs, said n being a positive integer including zero; and

a predetermined number of rows, said columns and rows together forming said array.

33. The array of claim 32 wherein said predetermined number of columns is 1920 and said predetermined number of rows is 1080.

34. The array of claim 32 wherein each of said first, second, third, and fourth group of columns including 480 columns.

35. The array of claim 32 wherein each of said first, second, third and fourth inputs are the same.

36. An active pixel matrix array for use in a microdisplay of a video projection system, comprising:

a predetermined number of columns, said columns divided into an upper section and a lower section; and

a predetermined number of rows, said columns and rows together forming said array.

37. The array of claim 36 wherein said upper section columns are configured to address a first group of rows and said lower section columns are configured to address a second group of rows, said first and second group of rows comprising said predetermined number of rows.

38. The array of claim 36 wherein said predetermined number of columns is 1920 and said predetermined number of rows is 1080.

39. The array of claim 36 wherein said predetermined columns are divided substantially

in the middle such that each of said upper section columns and each of said lower section columns have substantially the same length.

40. The array of claim 36 wherein said predetermined number of rows are divided into a left section and a right section.

41. The array of claim 40 wherein said left section rows include 540 rows and said right section rows include 540 rows.

42. The array of claim 40 wherein a first portion of said upper section columns are configured to address a first portion of said left section rows, a first portion of said lower section columns are configured to address a second portion of said left section rows, a first portion of said lower section columns are configured to address a first portion of said right section rows, and a second portion of said lower section columns are configured to address a second portion of said right section rows.

43. The array of claim 42 wherein said first and second portions of said upper section columns are non-overlapping, said first and second portions of said lower section columns are non-overlapping, said first and second portions of said left section rows are non-overlapping and said first and second portions of said right section rows are non-overlapping.

44. The array of claim 43 wherein said first and second portions of said upper section columns each includes 960 columns, wherein said first and second portions of said lower section columns each includes 960 columns, wherein said first and second portions of left section rows each includes 540 rows, and further, wherein said first and second portions of said right section rows each includes 540 rows.

45. A method of providing a pixel array for use in a microdisplay of a video projection

system, comprising the steps of:

depositing an underlying layer on a substrate layer;

depositing a dielectric layer on said underlying layer and polishing said dielectric layer to provide a substantially smooth upper surface; and

depositing a metal layer on said polished smooth upper surface of said dielectric layer and polishing said metal layer to provide a substantially smooth upper surface.

46. The method of claim 45 wherein said substrate layer includes a silicon substrate layer.

47. The method of claim 45 wherein said metal layer includes an aluminum layer.

48. The method of claim 45 wherein said step of polishing said upper surface of said metal layer includes the step of chemical mechanical polishing.

49. The method of claim 45 wherein said polished substantially smooth upper surface of said metal layer is configured to provide a high specular reflectivity.

50. A method of providing a pixel array for use in a microdisplay of a video projection system, comprising the steps of:

depositing an underlying layer on a substrate layer;

depositing a dielectric layer on said underlying layer and etching said dielectric layer on an upper surface to form a plurality of pixel grooves; and

depositing a metal layer on said etched upper surface of said dielectric layer and polishing said metal layer to provide a substantially smooth upper surface such that said metal layer is provided in said pixel grooves and an interpixel gap of said dielectric layer is provided between each adjacent pixel groove.

51 The method of claim 50 wherein said dielectric layer is substantially transparent.

52. The method of claim 51 wherein said dielectric layer has a high breakdown voltage.

53. A method of providing a pixel array for use in a microdisplay of a video projection system, comprising the steps of:

depositing an underlying layer on a substrate layer;

depositing a dielectric layer on said underlying layer;

depositing a metal layer on said dielectric layer; and

depositing a reflection enhancing layer on said metal layer.

54. The method of claim 53 wherein said reflection enhancing layer includes a coating comprising a stack of thin films.

55. The method of claim 53 wherein said reflection enhancing layer depositing step includes the steps of:

depositing a first silicon dioxide layer on said metal layer;

depositing a silicon nitride layer on said first silicon dioxide layer; and

depositing a second silicon dioxide layer on said silicon nitride layer.

56. The method of claim 55 wherein each of said first and second silicon dioxide layers and said silicon nitride layer has a thickness of half the wavelength of light divided by an index of refraction of said corresponding layers.

57. A method of providing an active pixel matrix array for use in a microdisplay of a video projection system, comprising the steps of:

providing a predetermined number of columns including even numbered columns and odd numbered columns, each of said even numbered columns configured to receive a first input, and each of said odd numbered columns configured to receive a second input; and

providing a predetermined number of rows, said columns and rows together forming said array.

58. The method of claim 57 wherein said predetermined number of columns is 1920 and said predetermined number of rows is 1080.

59. The method of claim 57 wherein said even numbered columns includes 960 columns and said odd numbered columns includes 960 columns, each of said even numbered columns adjacent to a respective odd numbered column.

60. A method of providing an active pixel matrix array for use in a microdisplay of a video projection system, comprising the steps of:

dividing a predetermined number of columns into an upper section and a lower section; and

providing a predetermined number of rows, said columns and rows together forming said array.

61. The method of claim 60 wherein said upper section columns are configured to address a first group of rows and said lower section columns are configured to address a second group of rows, said first and second group of rows comprising said predetermined number of rows.

62. The method of claim 60 wherein said predetermined number of columns is 1920 and said predetermined number of rows is 1080.

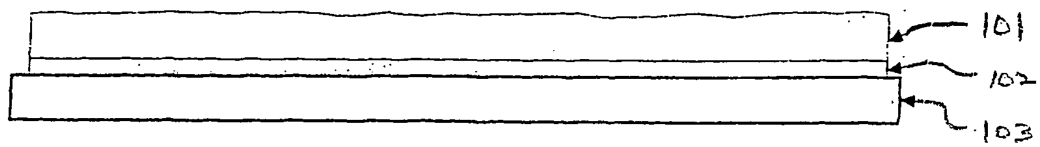


FIGURE 1A

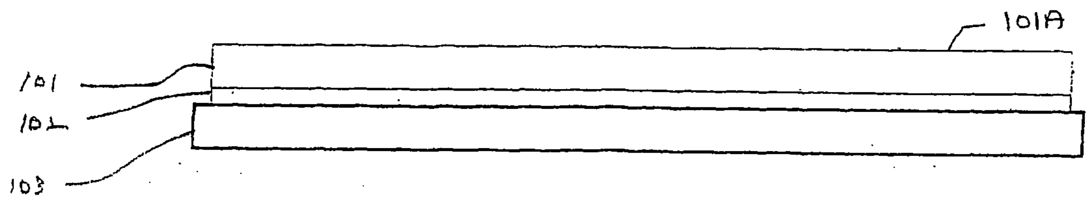


FIGURE 1B

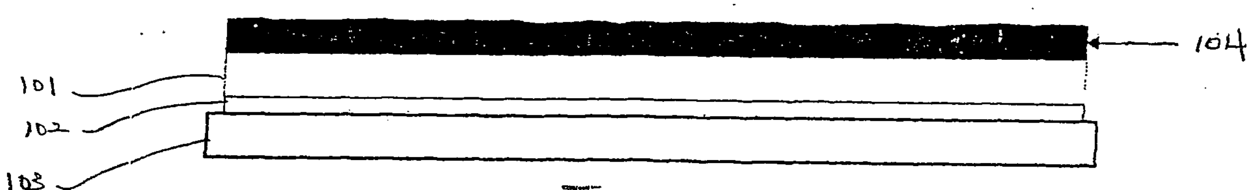


FIGURE 1C

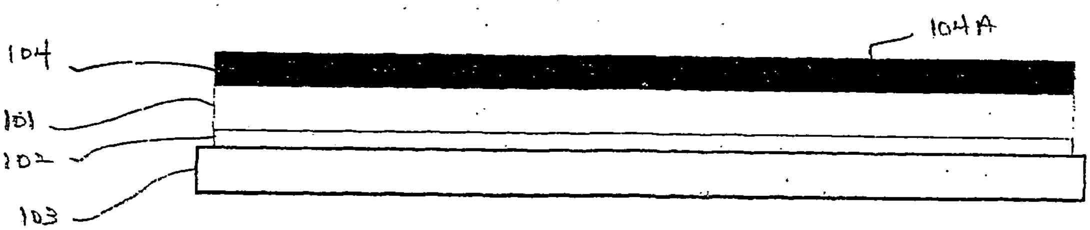


FIGURE 1D

FIGURE 2A

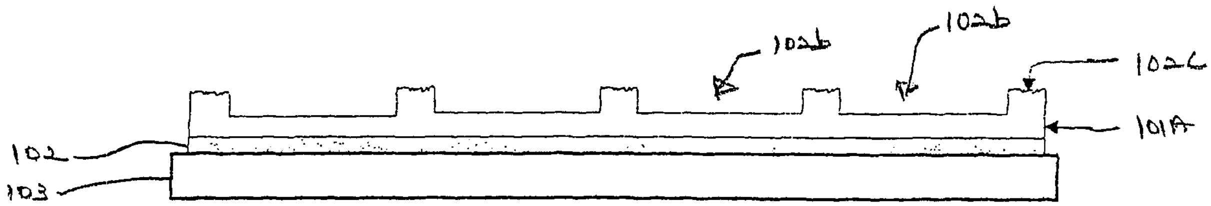


FIGURE 2B

FIGURE 2C

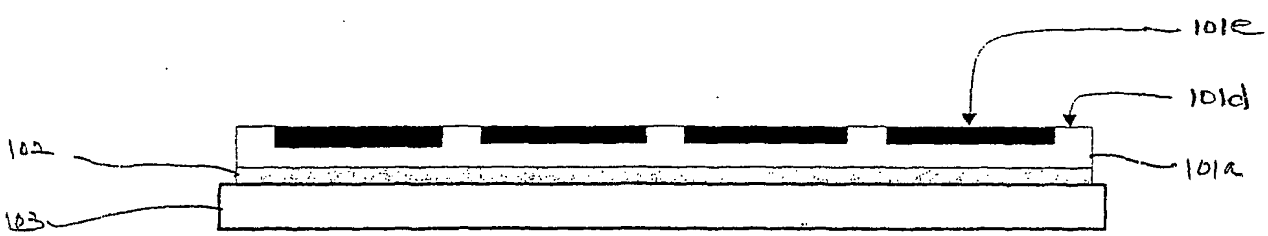


FIGURE 2D

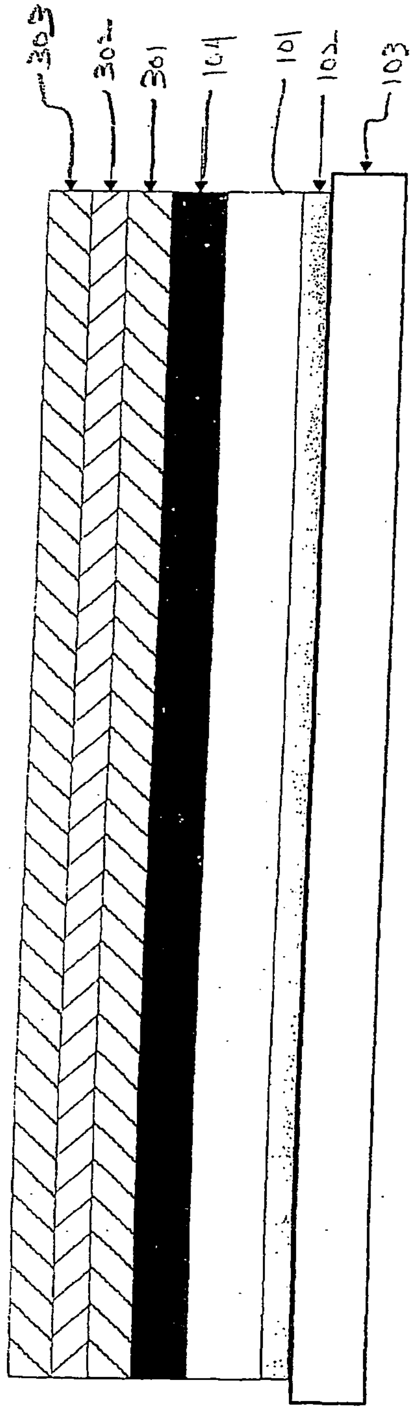


FIGURE 3

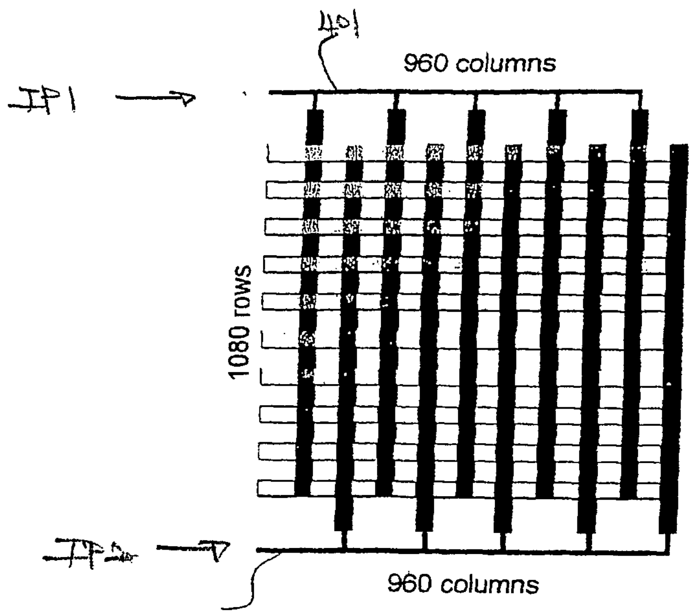


FIGURE 4A

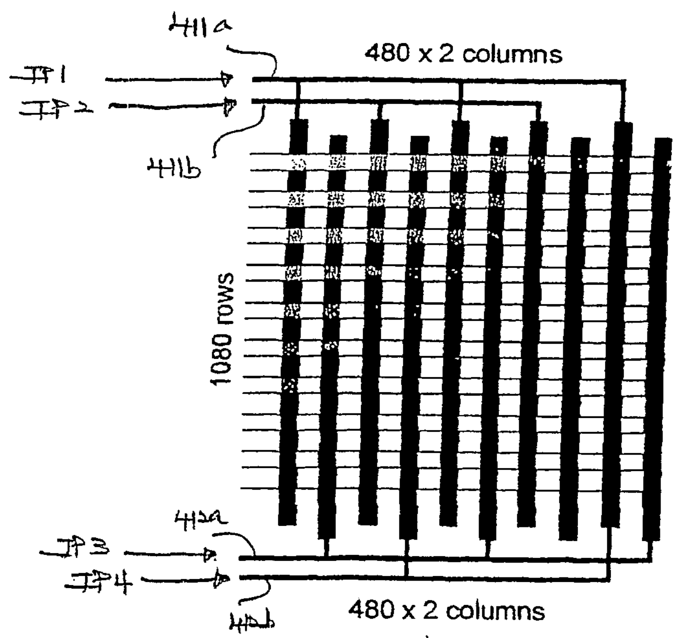


FIGURE 4B

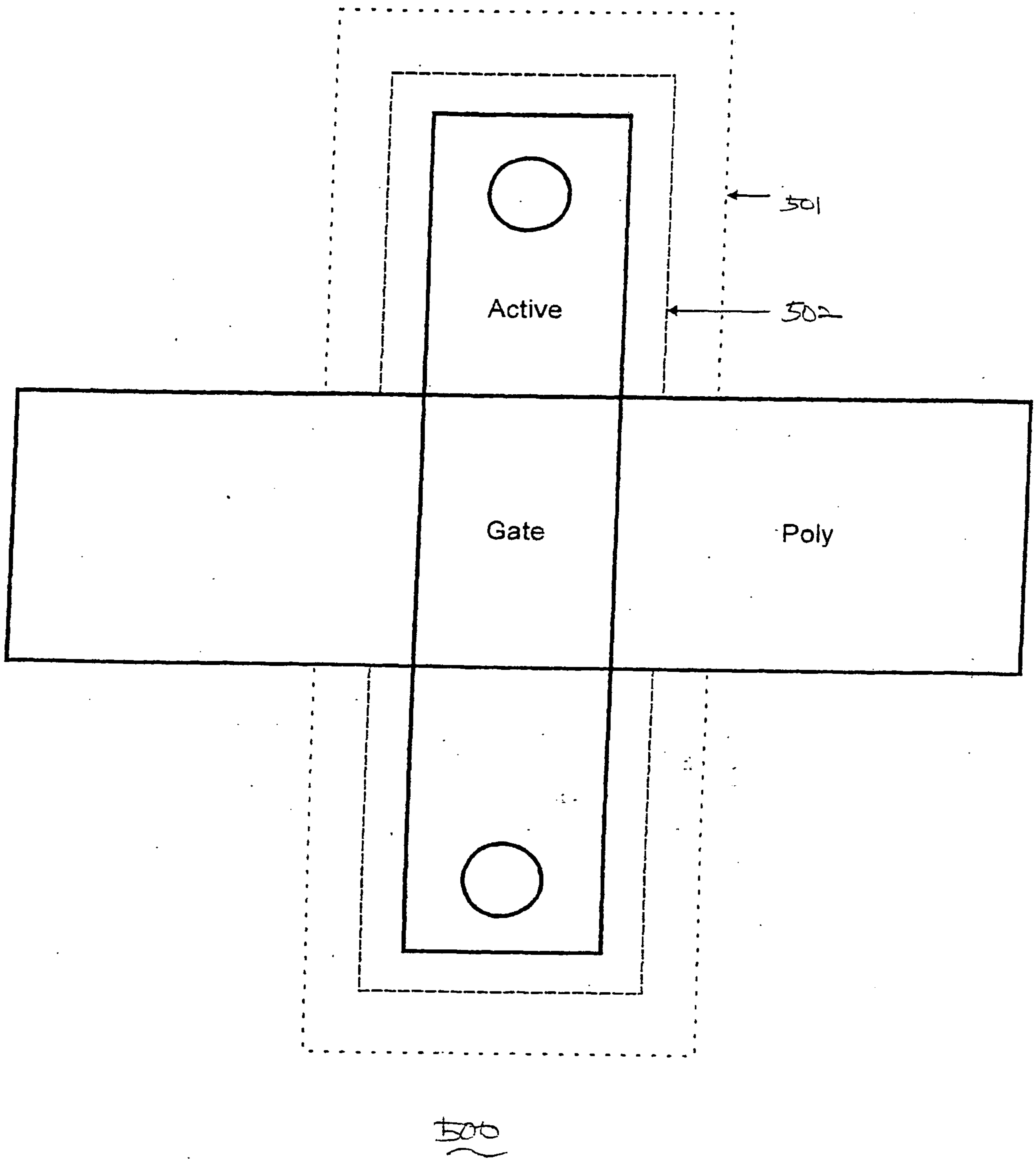


FIGURE 5

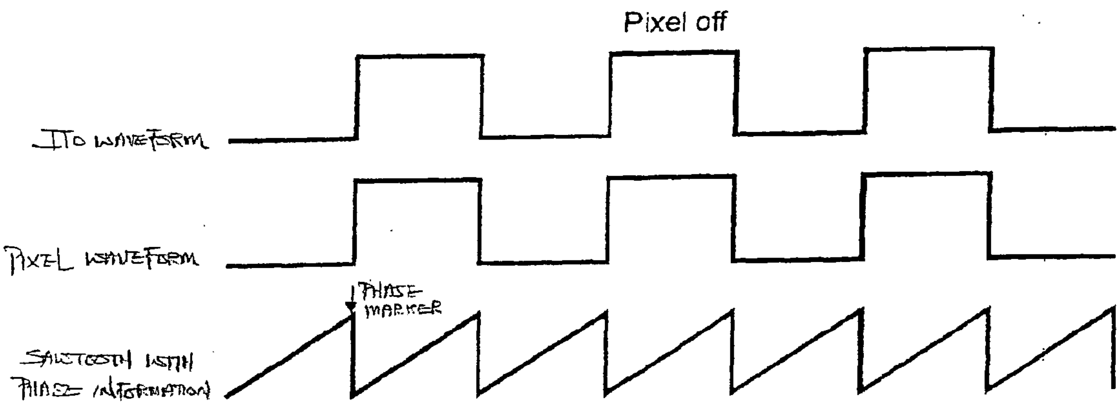


FIGURE 6A

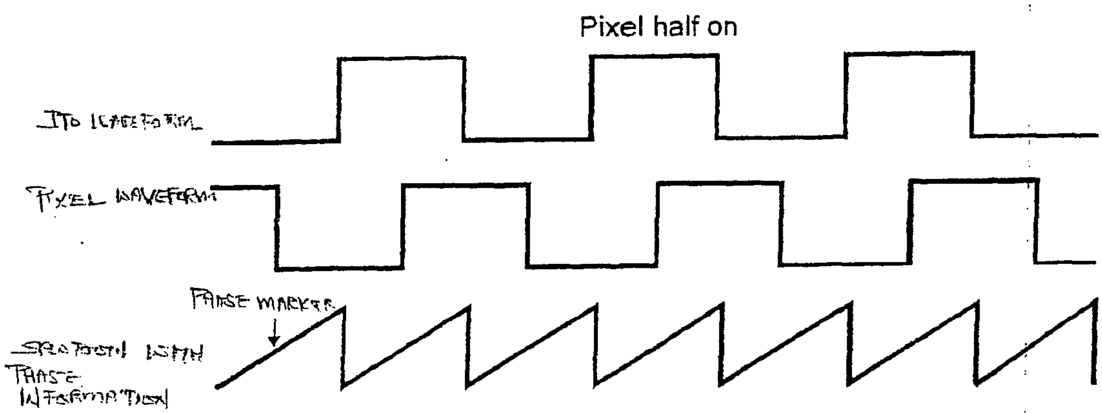


FIGURE 6B

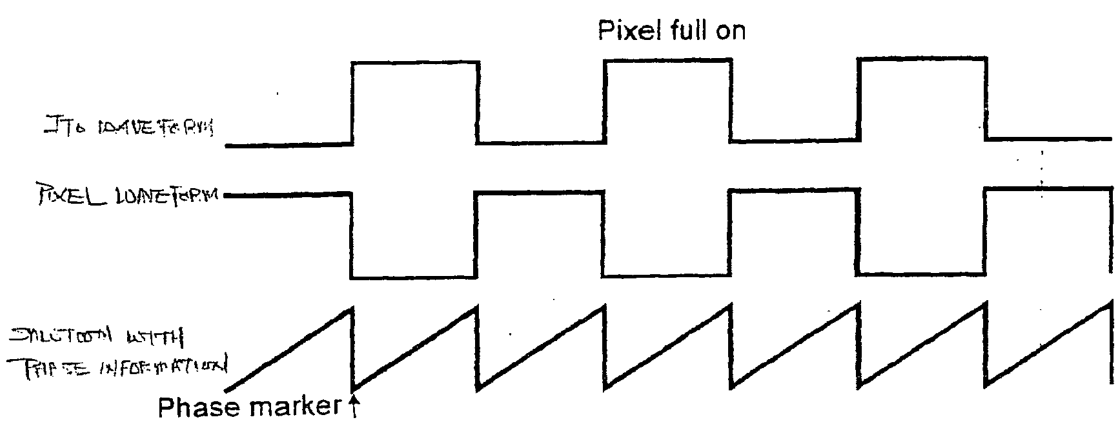


FIGURE 6C

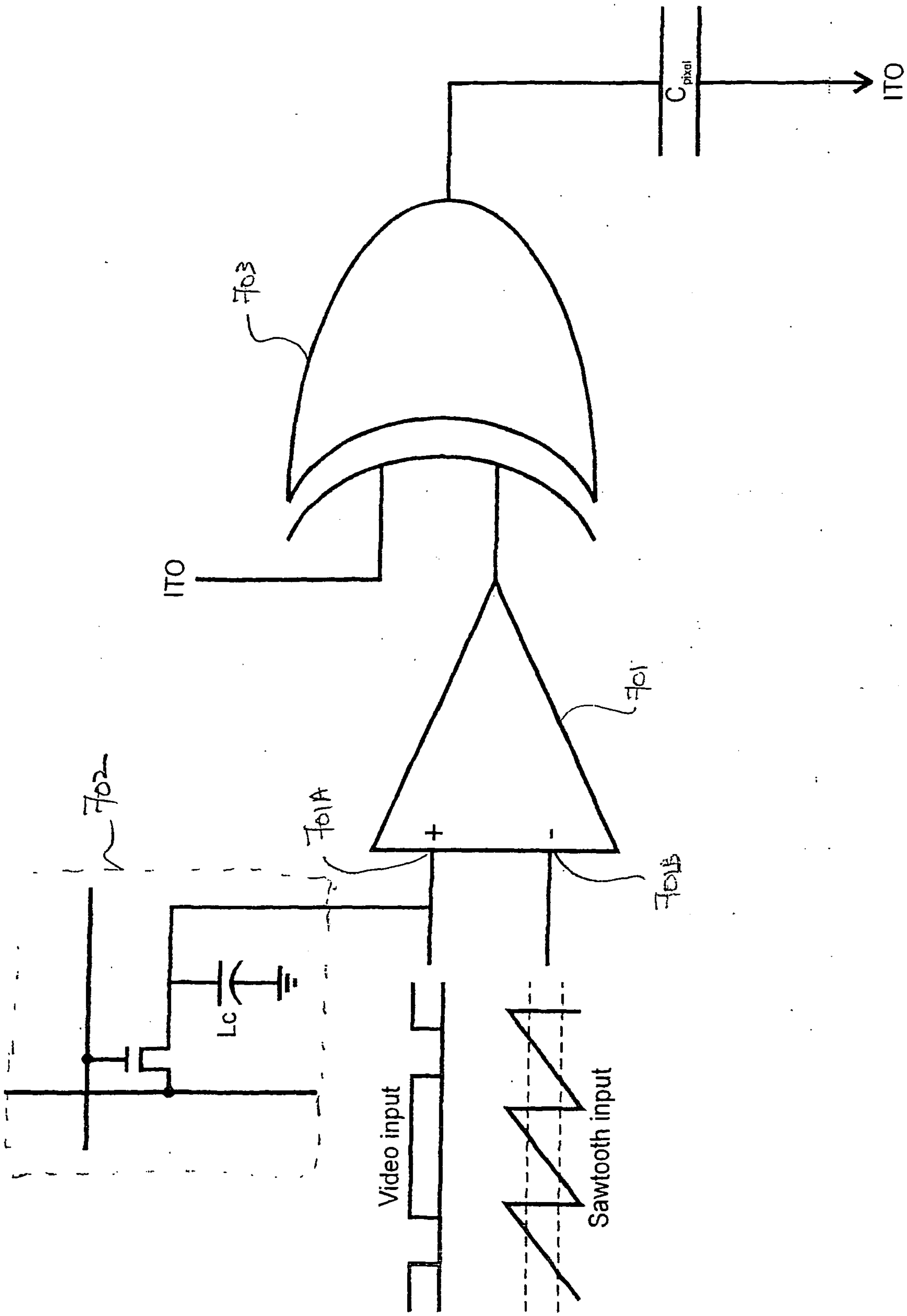

ITO
C_{pixel}
ITO
703
701
702
701A
701B
+
-
Lc
Video input
Sawtooth input

FIGURE 7

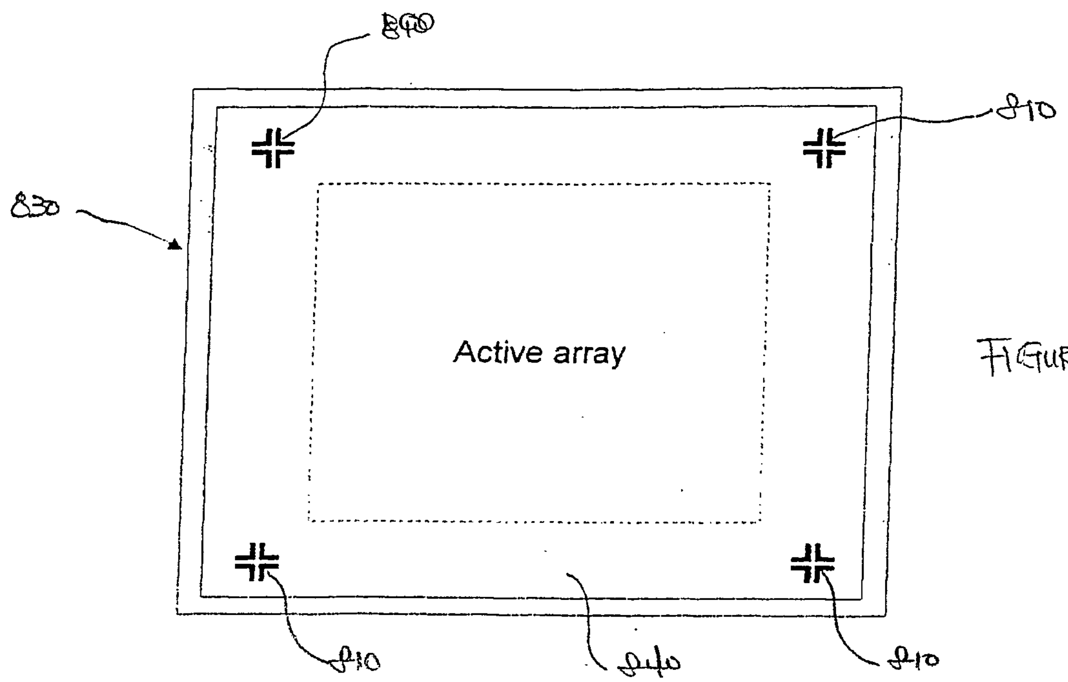


FIGURE 8A

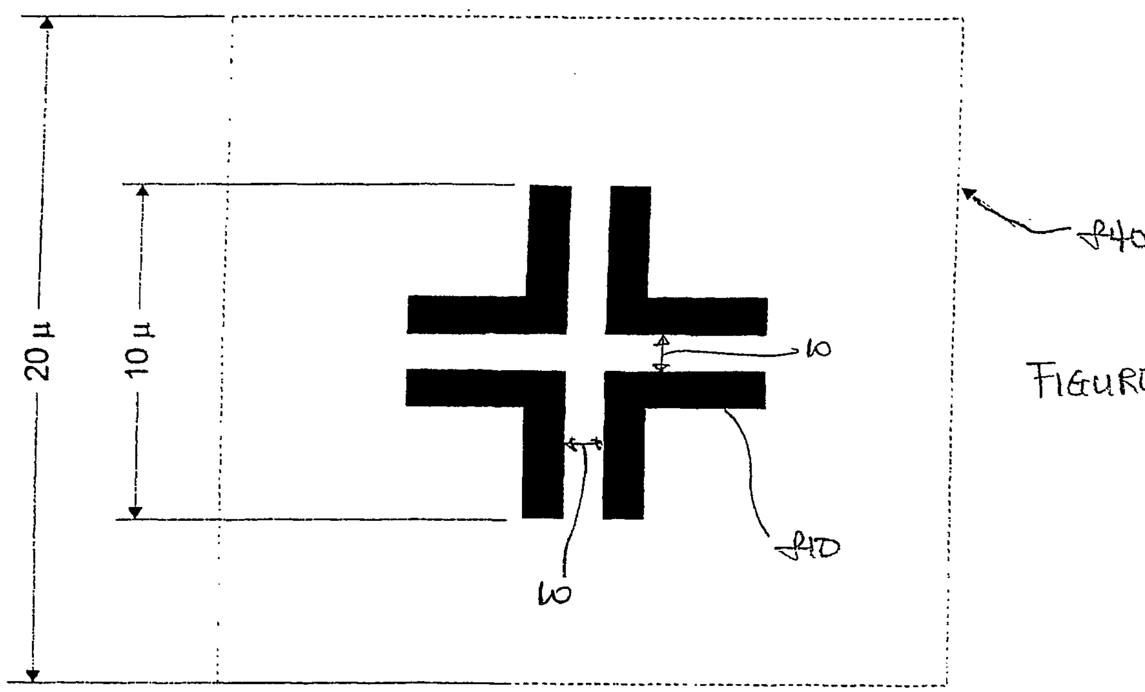


FIGURE 8B

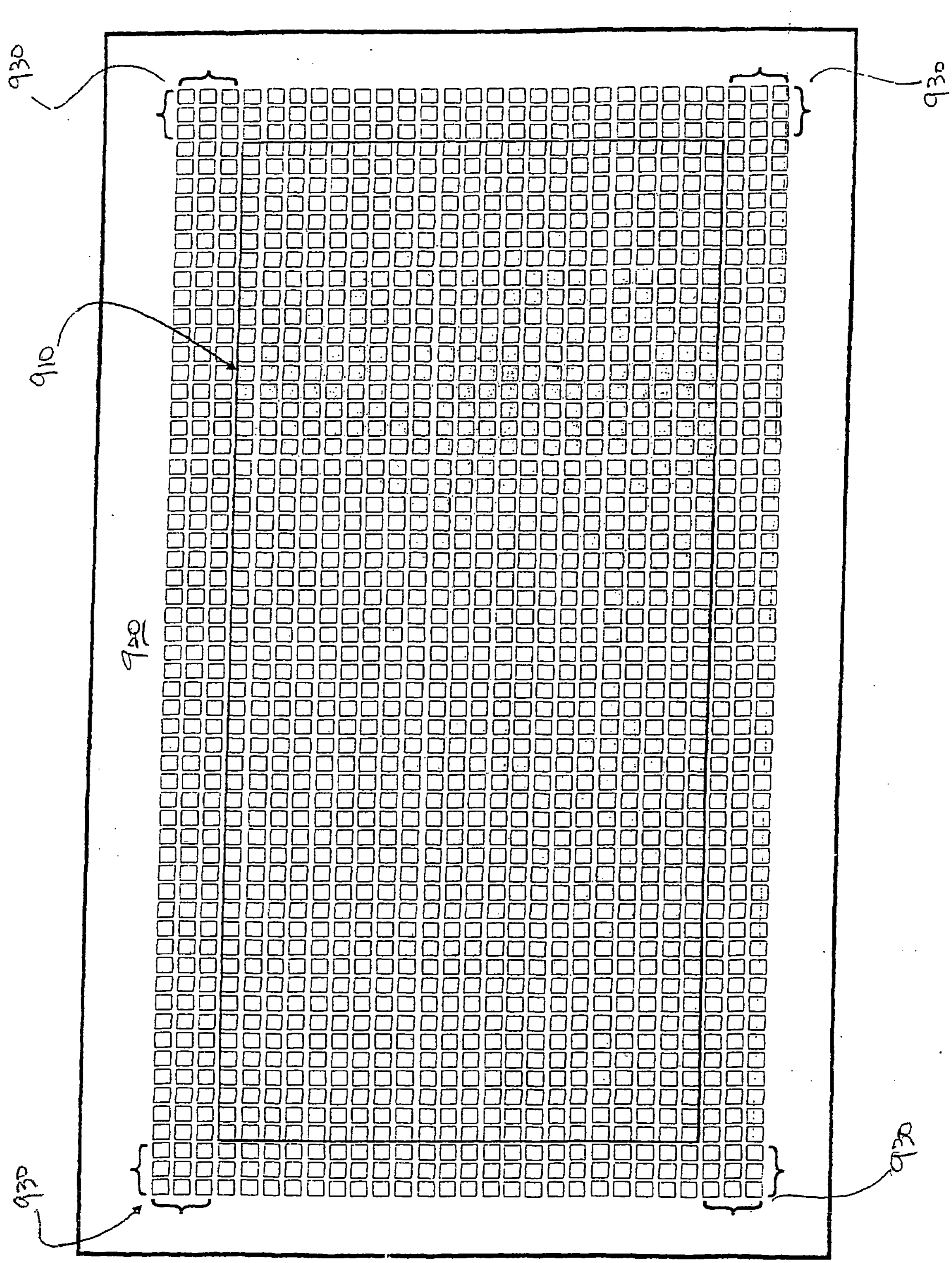


FIGURE 9

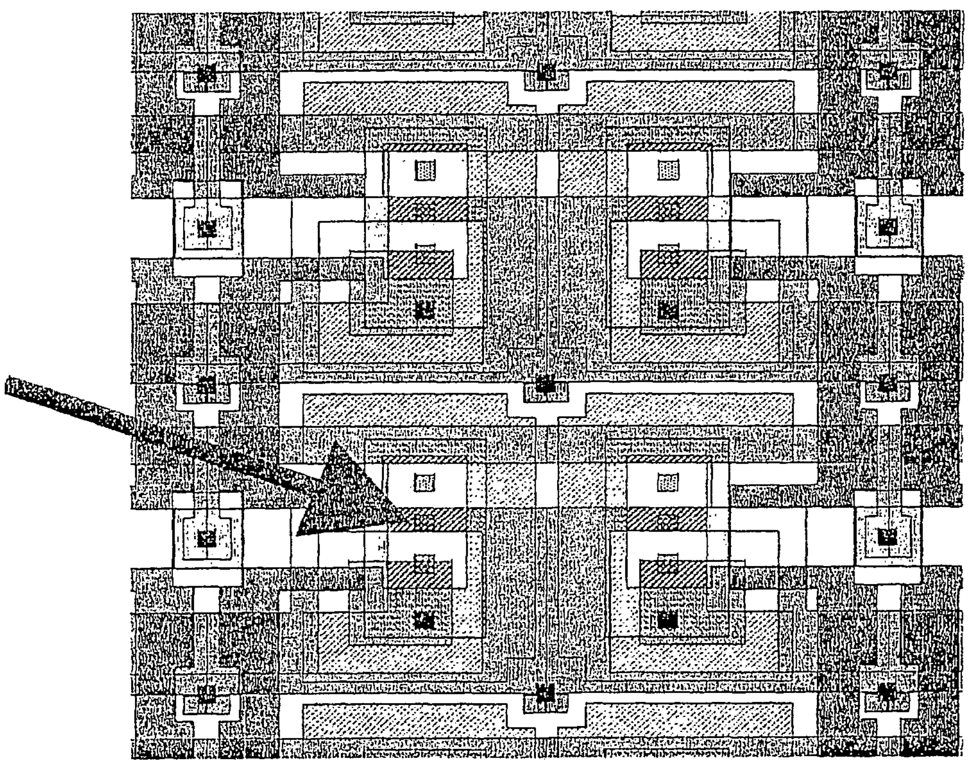


FIGURE 10

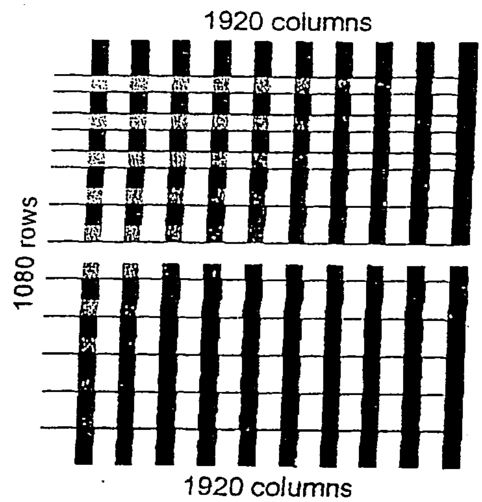


FIGURE 11A

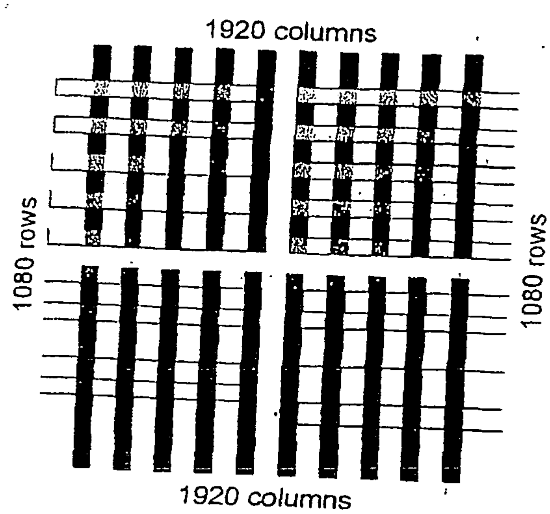


FIGURE 11B

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 December 2001 (13.12.2001)

PCT

(10) International Publication Number
WO 01/095619 A3

(51) International Patent Classification[7]: G02F 1/1335

(21) International Application Number: PCT/US01/18597

(22) International Filing Date: 7 June 2001 (07.06.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/210.284 8 June 2000 (08.06.2000) US

(71) Applicant: DIGITAL REFLECTON, INC. [US/US]; 644 University Avenue, Los Gatos, CA 95032 (US).

(72) Inventors: FLASCK, Richard; 10045 Nantucket, San Ramon, CA 94583-2865 (US). SANDBERG, Edmund; 17990 Rose Court, Monte Sereno, CA 95030 (US). PRIOR, Gregory, A.; 2814 Glen Heather Drive, San Jose, CA 95133 (US). WEIHS, Paul, J.; 37569 Summer Holly Common, Fremont, CA 94536 (US). CACHARELIS, Philip, John; 217 O'Connor, Menlo Park, CA 94025 (US).

(74) Agent: OH, Seong-Kun; Sierra Patent Group, Ltd., P.O. Box 6149, Stateline, NV 89449 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

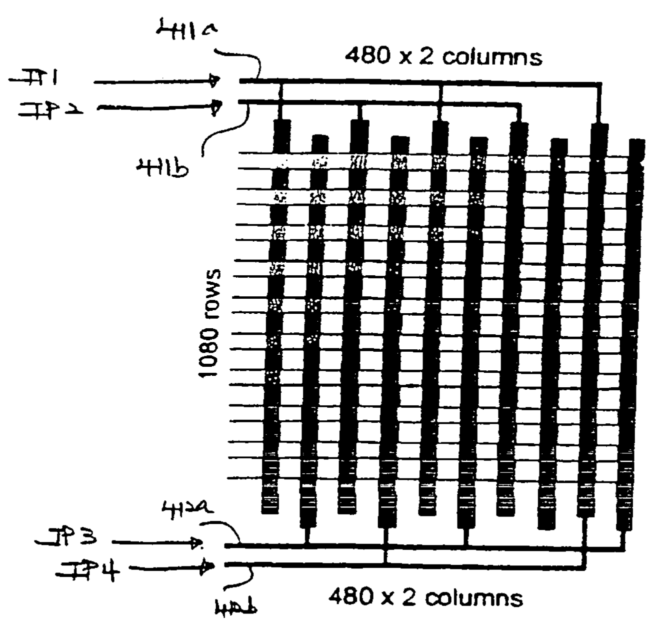
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report: 18 July 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: ACTIVE MATRIX SILICON SUBSTRATE FOR LCOS MICRODISPLAY



(57) Abstract: Method and system for providing improved performance of silicon substrate in a Liquid Crystal On Silicon (LCOS) microdisplay for use in video projection system with increased substrate reflectivity, reduced substrate scattering and diffraction, flicker suppression, minimized artifact of fringing and improved spatial uniformity of the gray scale, and allowing the substrate to operate in a high light environment is provided.

WO 01/095619 A3

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/18597

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G02F1/1335

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 837 354 A (CANON KK) 22 April 1998 (1998-04-22) column 9, line 08 -column 10, line 39; figure 1 ---	1-6, 45-49
X	EP 0 751 417 A (CANON KK) 2 January 1997 (1997-01-02) column 6, line 15 -column 7, line 27 ---	7-13, 50-52
X	US 5 767 827 A (KOBAYASHI TATSURU ET AL) 16 June 1998 (1998-06-16) column 4, line 37 -column 5, line 40 --- -/--	1-6, 45-49

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 February 2002	10.05.02

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	DIOT, P

Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
PCı/US 01/18597

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	O'HARA T ET AL: "FABRICATION OF SPATIAL LIGHT MODULATOR BACKPLANES USING DAMASCENE PROCESSING" PROCEEDINGS OF THE SPIE, SPIE, BELLINGHAM, VA, US, vol. 3292, 28 January 1998 (1998-01-28), pages 107-115, XP001034711 Chapters 4-6 ---	1-7, 45-50
X	US 6 037 197 A (HIRAKATA YOSHIHARU ET AL) 14 March 2000 (2000-03-14) column 6, line 52 -column 7, line 25 ---	1-6, 45-49
X	HUANG H C ET AL: "PLANARIZATION OF LIQUID-CRYSTAL-ON-SILICON PROJECTION DISPLAY WITH MULTILEVEL METALLIZATION AND CHEMICAL-MECHANICAL POLISHING" SID INTERNATIONAL SYMPOSIUM. DIGEST OF TECHNICAL PAPERS. SAN DIEGO, MAY 12 - 17, 1996, SANTA ANA, SID, US, vol. 27, 12 May 1996 (1996-05-12), pages 685-688, XP000621069 ISSN: 0097-966X the whole document ---	1-6
A	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 03, 29 March 1996 (1996-03-29) -& JP 07 294958 A (SEIKO INSTR INC), 10 November 1995 (1995-11-10) abstract; figure 5 ---	1,7,45, 50
A	PATENT ABSTRACTS OF JAPAN vol. 015, no. 487 (P-1286), 10 December 1991 (1991-12-10) -& JP 03 211528 A (MATSUSHITA ELECTRIC IND CO LTD), 17 September 1991 (1991-09-17) abstract; figure 2 -----	7

INTERNATIONAL SEARCH REPORT

I national application No.
PCT/US 01/18597

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-13,45-52

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-13,45-52

   A pixel array comprising a substrate layer (103) an underlying layer (102) deposited on said substrate layer; a dielectric layer (101) deposited on said underlying layer, said dielectric layer polished to provide a substantially smooth upper surface; and a metal layer deposited on said polished smooth upper surface of said dielectric layer, said metal layer polished to provide a substantially smooth upper surface.

2. Claims: 14-19,53-56

   A pixel array comprising: a substrate layer (103) an underlying layer (102) deposited on said substrate layer; a dielectric layer (101) deposited on said underlying layer; a metal layer deposited on said dielectric layer; and a reflection enhancing layer deposited on said metal layer.

3. Claims: 20-31 and 32-35, 57-59

   An active pixel matrix array comprising : a predetermined number of columns including even numbered columns and odd numbered columns (or first, second, third and fourth) , each of said even numbered columns configured to receive a first input, and each of said odd numbered columns configured to receive a second input; and a predetermined number of rows, said columns and rows together forming said array.

4. Claims: 36-44,60-62

   An active pixel matrix array comprising : a predetermined number of columns, said columns divided into an upper section and a lower section; and a predetermined number of rows, said columns and rows together forming said array.

INTERNATIONAL SEARCH REPORT

Iormation on patent family members

International Application No
PC1/US 01/18597

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0837354	A	22-04-1998	JP 3188411 B	16-07-2001
			JP 10177169 A	30-06-1998
			CN 1191323 A	26-08-1998
			KR 254326 B	01-05-2000
			US 6166792 A	26-12-2000
EP 0751417	A	02-01-1997	JP 3108861 B	13-11-2000
			JP 9073103 A	18-03-1997
			EP 1148374 A	24-10-2001
			KR 270129 B	16-10-2000
			US 5933204 A	03-08-1999
US 5767827	A	16-06-1998	JP 2864464 B	03-03-1999
			JP 8179377 A	12-07-1996
US 6037197	A	14-03-2000	JP 11031823 A	02-02-1999
JP 07294958	A	10-11-1995	NONE	
JP 03211528	A	17-09-1991	JP 2715612 B	18-02-1998